Please substitute the following paragraph for the paragraph beginning on page 6, line 17:

--U.S. Patent Application 09/176,022, titled, "Method and System for Down-Converting Electromagnetic Signals," (now U.S. Patent No. 6,061,551; hereinafter referred to as the '551 patent) incorporated herein by reference in its entirety, discloses methods and systems for directly down-converting EM signals.--

Please substitute the following paragraph for the paragraph beginning on page 6, line 21:

--The '551 patent discloses, among other things, how modulated EM signals can be directly down-converted to demodulated baseband information signals (also referred to interchangeably herein as direct to data or D2D embodiments). For example, amplitude modulated (AM) signals and phase modulated (PM) signals can be directly down-converted to demodulated baseband information signals by aliasing the AM and PM signals at sub-harmonics of the AM and PM signals.--

Please substitute the following paragraph for the paragraph beginning on page 7, line 5:

--Frequency modulated (FM) signals, however, pose special challenges. For example, the '551 patent discloses how frequency shift keying (FSK) signals, when aliased at a fixed sub-harmonic, are down-converted to amplitude shift keying signals or to phase shift keying (PSK) signals. FM signals, unlike AM and PM signals, are not necessarily directly down-converted to demodulated baseband information signals by aliasing at a fixed sub-harmonic.--

Please substitute the following paragraph for the paragraph beginning on page 7, line 21:

--The zero IF FM decoder 502 includes a first aliasing module 510 and a second aliasing module 512. Preferably, the first and second aliasing modules 510 and 512 are implemented as disclosed in the '551 patent and may be optimized as illustrated in FIGS. 1-3

a5 of the present application and as described above. Other components of the zero IF FM decoder 502 are described below with the description of the process flowchart 402.--

Please substitute the following paragraph for the paragraph beginning on page 8, line 4:

a6 --In FIG. 5, step 410 is performed by the first and second aliasing module 510 and 512. The first aliasing module 510 receives an FM signal 514 and a first LO signal 516. The first LO signal 516 is substantially equal to the frequency of the FM signal 514 or a sub-harmonic thereof. Details of maintaining the LO signal 516 at the frequency of the FM signal 514, or a sub-harmonic thereof, is described in connection with step 412 below. The first aliasing module 510 uses the first LO signal 516 to down-convert the FM signal 514 to a first down-converted signal 518, as disclosed in the '551 patent.--

Please substitute the following paragraph for the paragraph beginning on page 8, line 18:

a7 --In an exemplary embodiment, the first and second LO signals 516 and 520 are separated by 1/4 period of the FM signal 514, or any multiple of a period of the FM signal 514 plus 1/4 period. Other phase differences are contemplated and are within the scope of the present invention. The second aliasing module 512 uses the second LO signal 520 to down-convert the FM signal 514 to a second down-converted signal 522, as disclosed in the '551 patent.--

Please substitute the following paragraph for the paragraph beginning on page 8, line 27:

a8 --The '551 patent teaches that, so long as an aliasing rate remains substantially equal to the frequency of an FM signal, the resultant down-converted signal is substantially a constant level. In the case of the zero IF FM decoder 502, therefore, the first and second down-converted signals 518 and 522 should generally be constant signals.--

Please substitute the following paragraph for the paragraph beginning on page 12, line 12:

a9

--The present invention can be implemented with an aliasing system as disclosed in '551 patent, incorporated herein by reference in its entirety.--

Please substitute the following paragraph for the paragraph beginning on page 12, line 20:

a10

--The exemplary aliasing system 100 includes an aliasing module 110 that aliases an EM signal 112, using an aliasing signal 114, and outputs a down-converted signal 116, as disclosed in '551 patent, incorporated herein by reference in its entirety. The aliasing module 110 is also referred to herein as a universal frequency translator (UFT) module.--

Please substitute the following paragraph for the paragraph beginning on page 13, line 3:

a11

--Aliasing system 100 optionally includes one or more of an input impedance match module 118, a parallel resonant tank module 120, and an output impedance match module 122, as disclosed in the '551 patent.--

Please substitute the following paragraph for the paragraph beginning on page 14, line 8:

a12

--The exemplary schematic diagram 202 includes a storage module 210 for storing energy transferred from the EM signal 112, as disclosed in the '551 patent.--

Please substitute the following paragraph for the paragraph beginning on page 14, line 27:

--FIG. 3 illustrates an aliasing module 302, which is an exemplary embodiment of the aliasing module 110 and the ASIC 212. The aliasing module 302 includes a sine wave to square wave converter module 310, a pulse shaper module 312 and a switch module 314. The sine wave to square wave converter module 310 converts a sine wave 114 from the local oscillator 128 to a square wave 311. The pulse shaper module 312 receives the square wave 311 and generates energy transfer pulses 313 therefrom. Energy transfer pulses are discussed in greater detail in the '551 patent.--

a13

Please substitute the following paragraph for the paragraph beginning on page 18, line 14:

--In one implementation of the invention, switch 906 is a field effect transistor (FET). A specific implementation wherein the FET is a complementary metal oxide semiconductor (CMOS) FET is shown in FIG. 11. A CMOS FET has three terminals: a gate 1102, a source 1104, and a drain 1106. String of pulses 910 is shown at gate 1102, bias signal 814 is shown at source 1104, and rectangular waveform 834 is shown at drain 1106. Those skilled in the relevant art(s) will appreciate that the source and drain of a FET are interchangeable, and that bias signal 814 could bee at the drain 1106, with rectangular waveform 834 being at the source 1104. Numerous circuit designs are available to eliminate any possible asymmetry, and an example of such a circuit may be found in U.S. Patent No. 6,091,940, entitled "Method and System for Frequency Up-Conversion," the full disclosure of which is incorporated herein by reference.--

a14

Please substitute the following paragraph for the paragraph beginning on page 20, line 8:

--The inventions described above can be implemented individually. Alternatively, two or more of the inventions described above can be implemented in combination with one another. For example, one or both of the ultra-low power down-converter and zero IF FM decoder an be implemented with the high efficiency transmitter described above, as a transceiver. Also, one or both of the ultra-low power down-converter and zero IF FM

a15